Claims

1. A portable data storage device including:

(i) a data interface for transferring data packets into and out of the device;

(ii) an interface controller,

(iii) a master control unit, and

(iv) at least one NAND flash memory unit,

the interface controller being arranged to send data received through the interface to the master control unit, and

the master control unit being arranged to recognise certain data packets as encoding READ instructions and other data packets as encoding WRITE instructions:

(a) upon receiving a READ instruction indicating a logical address, to access a memory address mapping table which associates logical address regions within a logical memory space with respective first physical address regions within the memory unit, to read data from a physical address in the memory unit corresponding to the logical address according to the address mapping table, and to transmit to the data interface one or more data packets including the data which was read, and

(b) upon receiving a WRITE instruction indicating a logical address and data to be written to that logical address, to determine if the physical address corresponding to the logical address according to the memory address mapping table is in the erased state and:

if so, to write the data to that physical address, or

if not, to modify the address mapping table to associate a second physical address region with the logical address region containing the logical address, to write the data to a physical address corresponding to the logical address according to the modified memory address mapping table, and to copy any data stored in other potions of the first physical address region to corresponding locations of the second physical address region.

2. A device according to claim 1 in which data defining the memory address mapping table is stored as mapping data in the flash memory unit, the memory control device being arranged to modify the mapping data upon modifying the memory address mapping table.

3. A device according to claim 2 in which the memory control address unit is arranged, upon being initiated, to extract the mapping data from the flash memory unit and generate the memory address mapping table within RAM memory.

4. A device according to claim 2 or claim 3 in which the portion of the mapping data defining the mapping between each respective physical address region and a logical address region is stored within that physical address region.

5. A device according to claim 4 in which the mapping data relating to a given physical address region is stored in the control data storage sector of one or more pages of the physical address region.

6. A device according to any preceding claim in which the physical memory space includes:

(i) physical memory regions associated with logical address regions by the memory address mapping table, and

(ii) queuing physical memory regions which can become associated with the logical addresses under the operation of the master control unit which modifies the memory address mapping table.

7. A device according to claim 6 in which the queuing physical memory regions are in the erased state.

8. A device according to claim 6 or claim 7 in which the physical memory space further includes reserved physical memory regions which cannot become associated with the logical addresses under the operation of the master control unit which modifies the memory address mapping table.

9. A device according to any preceding claim in which the physical address regions are respective blocks of the memory unit.

10. A device according to any of claims 1 to 8 in which the physical address regions are groups of blocks in the memory unit, the groups being defined according to a grouping table.

11. A device according to claim 10 in which the majority of groups of blocks are defined according to a rule, and the grouping table defines groups which are exceptions to the rule.

12. A device according to claim 11 in which the memory address mapping table contains a flag in respect of any logical address region which is associated with one of the groups which are exceptions to the rule.

13. A device according to any of claims 10 to 12 in which the master control unit associates consecutively following logical addresses within a logical address region with respective pages in different ones of the blocks.

14. A device according to claim 13 in which the master control unit associates consecutive logical addresses into sets, each of the sets of logical

addresses having a number of members equal to the number of blocks in each group, and for each given set the master control unit associates the logical addresses of that set with corresponding pages of the respective blocks.

15. A device according to any preceding claim in which the master control unit is arranged, in response to receiving a first WRITE instruction to implement the write instruction only upon determining that, within a predefined period, a second WRITE instruction is not received obeying a predefined similarity criterion.

16. A device according to claim 15 in which, following a modification of the memory address modification table in relation to a given logical address region, and prior to said copying of the data from the first physical address region to the new second address region, said criterion is whether the second WRITE instruction relates to a logical address corresponding to the location within the given logical address region of the data to be copied, and in the case that such a WRITE instruction is received aborting said copying operation and instead writing data specified by the second WRITE instruction to the location of the second physical address region.

17. A device according to claim 15 in which the master control unit has access to a data cache and in response the first WRITE instruction writes the data to the data cache, said criterion being that the second WRITE instruction relates to the same logical address as the first instruction, in the case that the determination is positive the data specified in the second WRITE instruction being written to the data cache.

18. A device according to claim 15 in which the master control unit has access to a data cache and in response to the first WRITE instruction writes the data to the data cache provided that the WRITE instruction relates to one or more selected logical addresses, said criterion being that the second

WRITE instruction relates to the same logical address as the first instruction, in the case that the determination is positive the data specified in the second WRITE instruction being written to the data cache.

19. A device according to claim 18 in which there are a plurality of said selected logical addresses.

20. A device according to claim 18 or 19 further including a pattern recognition unit for recognising logical addresses encoded in the WRITE instructions which arise with relatively high frequency, and for setting said recognised logical addresses as said selected logical addresses.